RMo1B-1

A 4.2-9.2GHz Cryogenic Transformer Feedback Low Noise Amplifier with 4.5K Noise Temperature and Noise-Power Matching in 22nm CMOS FDSOI

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Outline

- Introduction
- Circuit Implementation
  - Simultaneous Noise and Power Matching
  - Transistor Optimization
  - Transformer Feedback
  - Cryogenic Applications
- Measurement Results
- Summary

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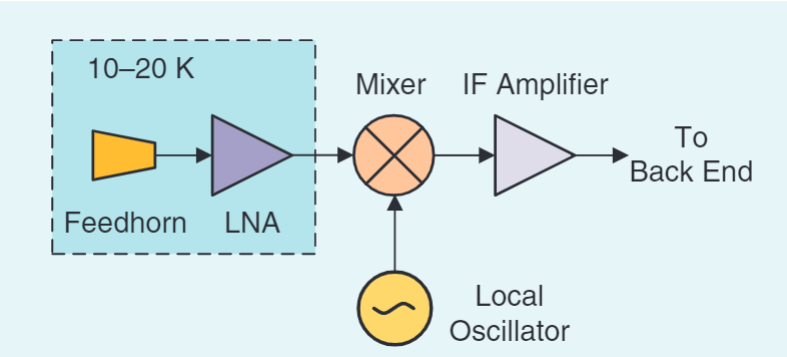
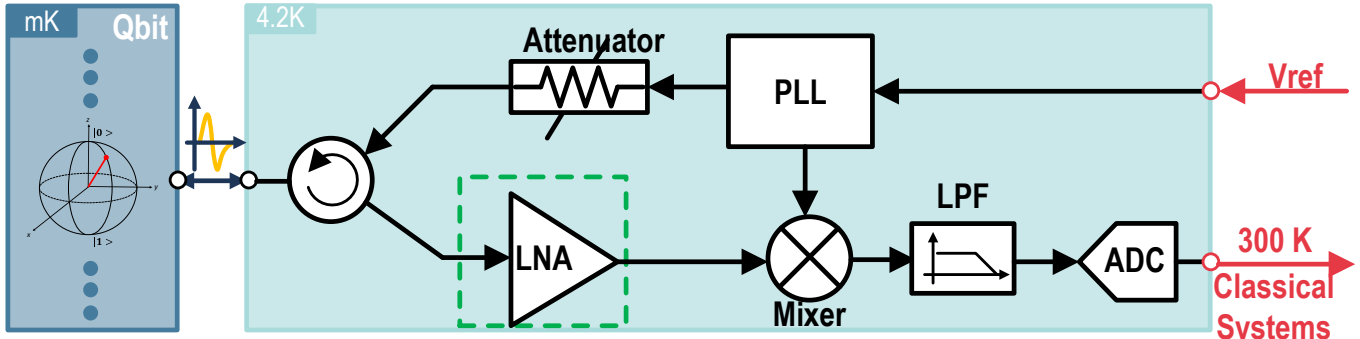
Introduction

- Cryogenic electronic circuits applications
  - ➢ Deep space applications, Planetary applications, Radioastronomy, …
  - ➢ Quantum computation applications

    → Classical electronic controller as intermediate interface between mK environment and room temperature environment



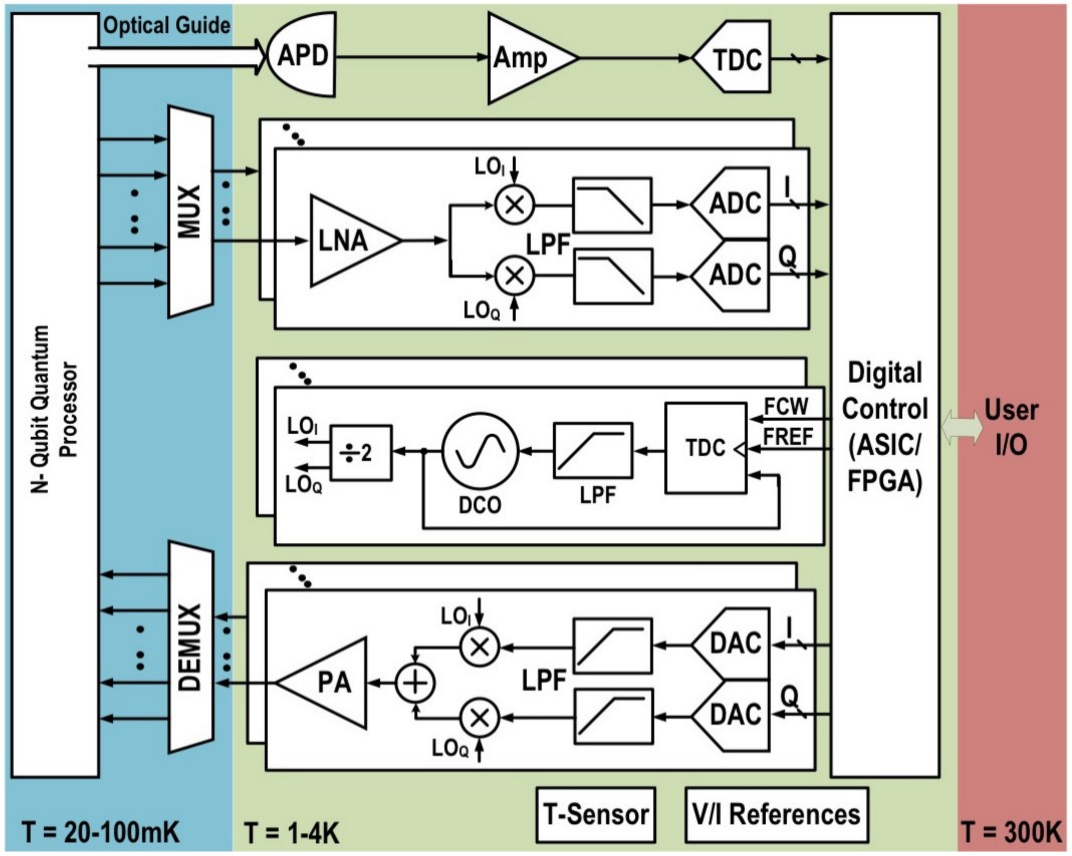
Typical receiver for radioastronomy[1]



Simplified System block diagram for the classical electronic controller for solid-state qubits

Introduction

- Cryogenic CMOS controller
  - → Existing large scale integration capability
  - → Compatible with semiconductor Qubits
- Cryogenic CMOS low noise amplifier (LNA)
  - Required in most of the read-out systems to amplify the extremely weak read-out signal
  - Frequency multiplex requires a broadband operation

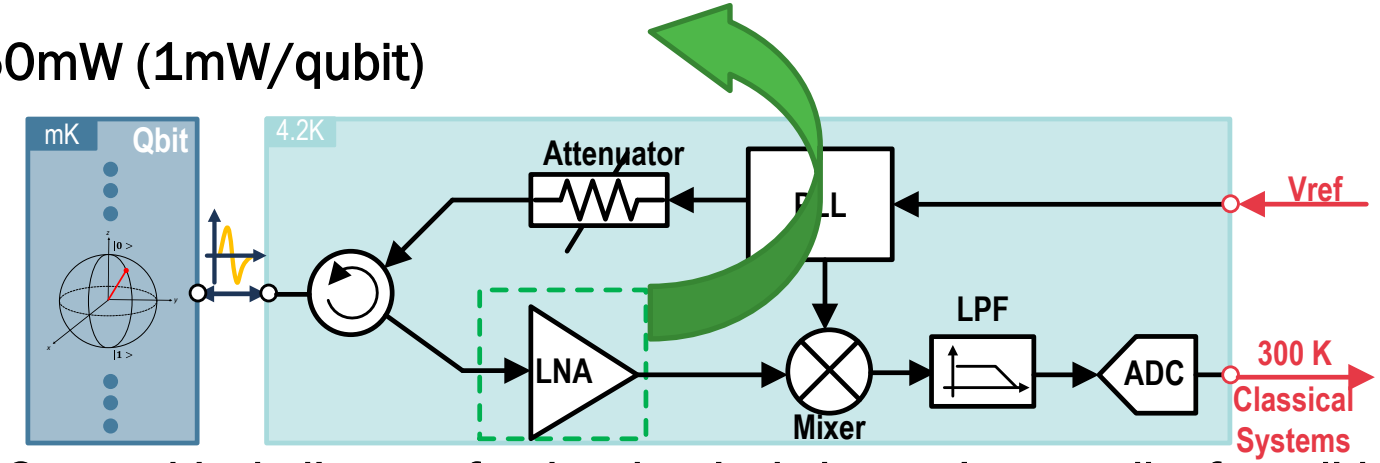


Example of multi-channel classical interface to a quantum processor. [2]

Introduction

- Cryogenic LNA specifications for gate dispersive qubits read-out [3]
  - ❑ Operation Frequency: 4GHz – 8GHz
  - ❑ Noise figure (NF): < 0.8 dB
  - ❑ Gain: > 40dB
  - ❑ Power: < 50mW (1mW/qubit)

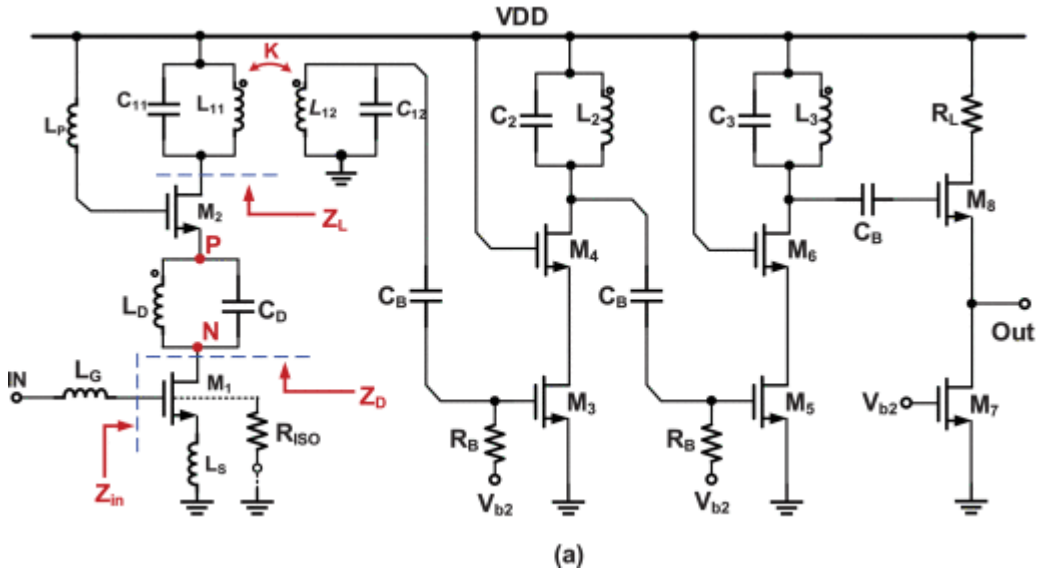
Broadband power-noise matching is needed



Simplified System block diagram for the classical electronic controller for solid-state Qubits

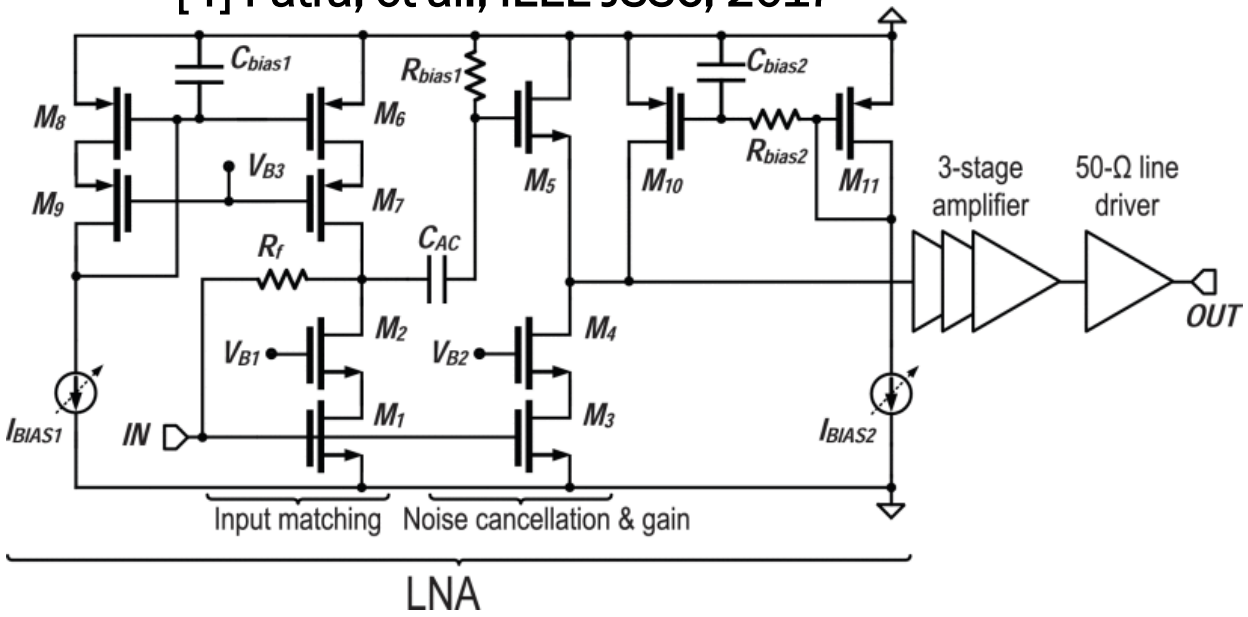
Prior State-of-the-Art CMOS LNA

[3] Peng, et al., IEEE JSSC, 2021



- Frequency: 4.6-8.2 GHz
- NF: 0.23-0.65dB
- Inductive degenerated Common source

[4] Patra, et al., IEEE JSSC, 2017



- Frequency: 0.1-0.5 GHz
- NF: 0.1-0.8dB
- Noise Canceling

No broadband simultaneous power-noise matching

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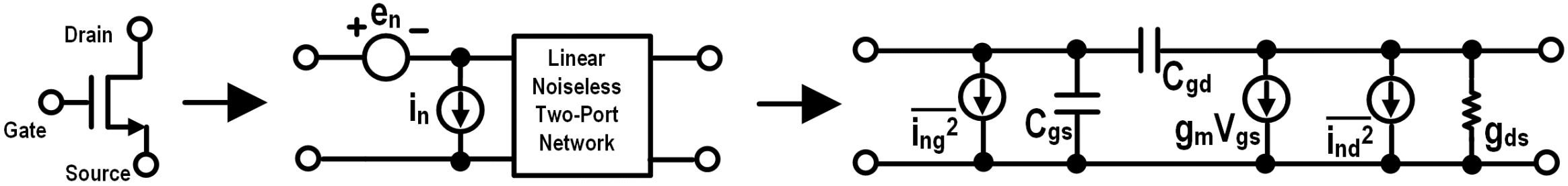
Simultaneous Power and Noise Matching



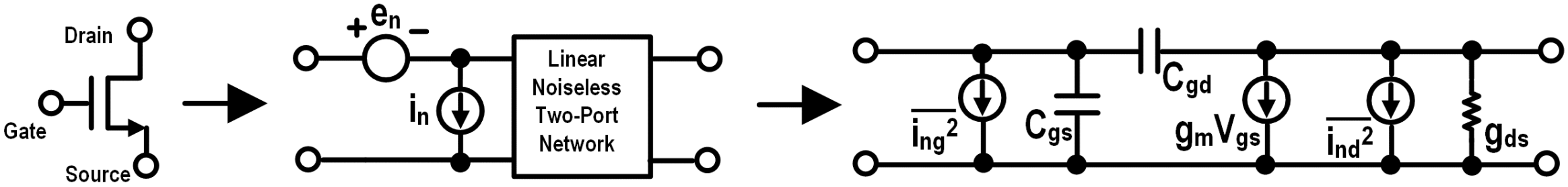
- Simple equivalent noise circuit for MOSFET device has been studied previously [5]
- Gate Induced Noise Current Source: $\overline{i_{ng}^2} = \frac{4kT\Delta f \delta \omega^2 C_{gs}^2}{5 g_{d0}}$
- Drain Noise Current Source: $\overline{i_{nd}^2} = 4kT\Delta f \gamma g_{d0}$
- Noise Source Correlation Coefficient: $c = \frac{\overline{i_{nd}^* i_{ng}}}{\sqrt{i_{nd}^2 i_{ng}^2}}$

δ: The Excess Gate Noise Coefficient

γ: The Excess Drain Noise Coefficient

$g_{d0} = \frac{g_m}{\alpha}$ is the output conductance when Vds = 0V

Simultaneous Power and Noise Matching

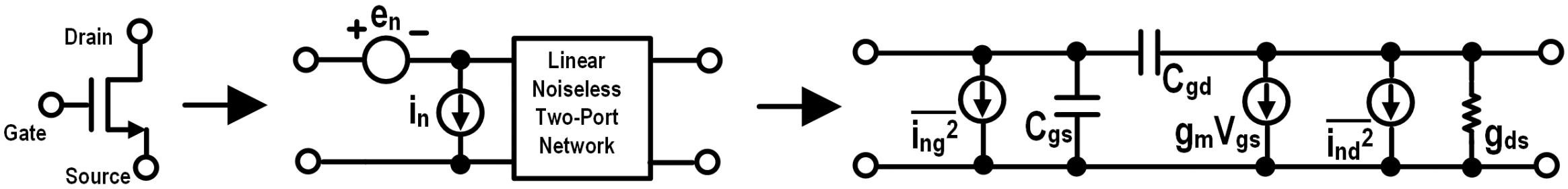


- As discussed in [6], this two-port network achieves the minimum noise figure when:

$$\begin{cases} G_{opt} = \omega C_{gs}\psi \\ B_{opt} = -\omega C_{gs}\xi \end{cases}, \quad Where \quad \psi = \alpha\sqrt{(1-|c|^2)\delta/5\gamma} \quad \xi = 1-\alpha|c|\sqrt{\delta/5\gamma}$$

- Achievable minimum Noise figure is independent of the value of source inductor

Simultaneous Power and Noise Matching



- [6] shows that simultaneous power and noise matching is achieved when:

$$\psi^2 + \xi^2 = \xi$$

- 22nm CMOS FDSOI has low intrinsic C_{gs} at frequency band of interests

→External Cgs is added to provide an additional degree of freedom

Design Flow

- The noise parameters are dependent of frequency
- We follow the following design procedures:

$$\begin{cases} G_{opt} = \omega(C_{gs,ext} + C_{gs,int})\psi \\ B_{opt} = -\omega(C_{gs,ext} + C_{gs,int})\xi \end{cases}$$

$C_{gs,ext}$ tuning

Obtain

$$\psi^2 + \xi^2 = \xi$$

Obtain

$$\begin{cases} C_{gs,ext} + C_{gs,int} \\ g_m \end{cases}$$

Obtain

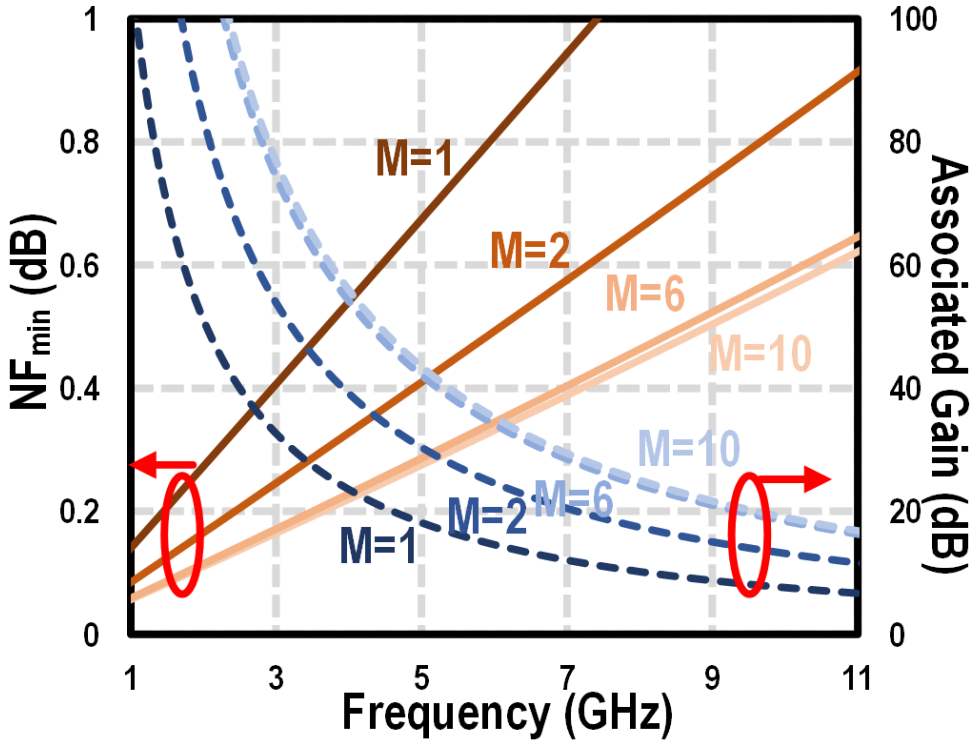
$$\psi = \alpha\sqrt{(1 - |c|^2)\delta/5\gamma}$$

$$\xi = 1 - \alpha|c|\sqrt{\delta/5\gamma}$$

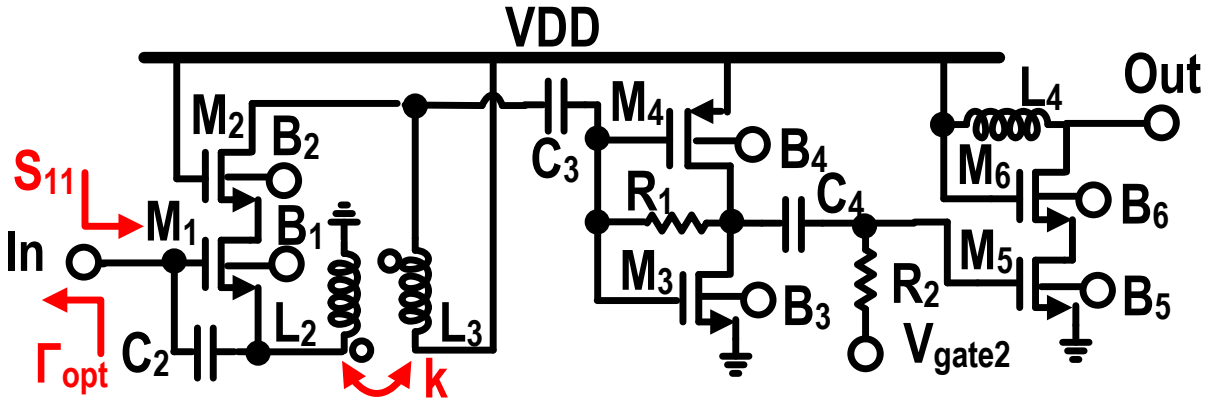
?Satisfy

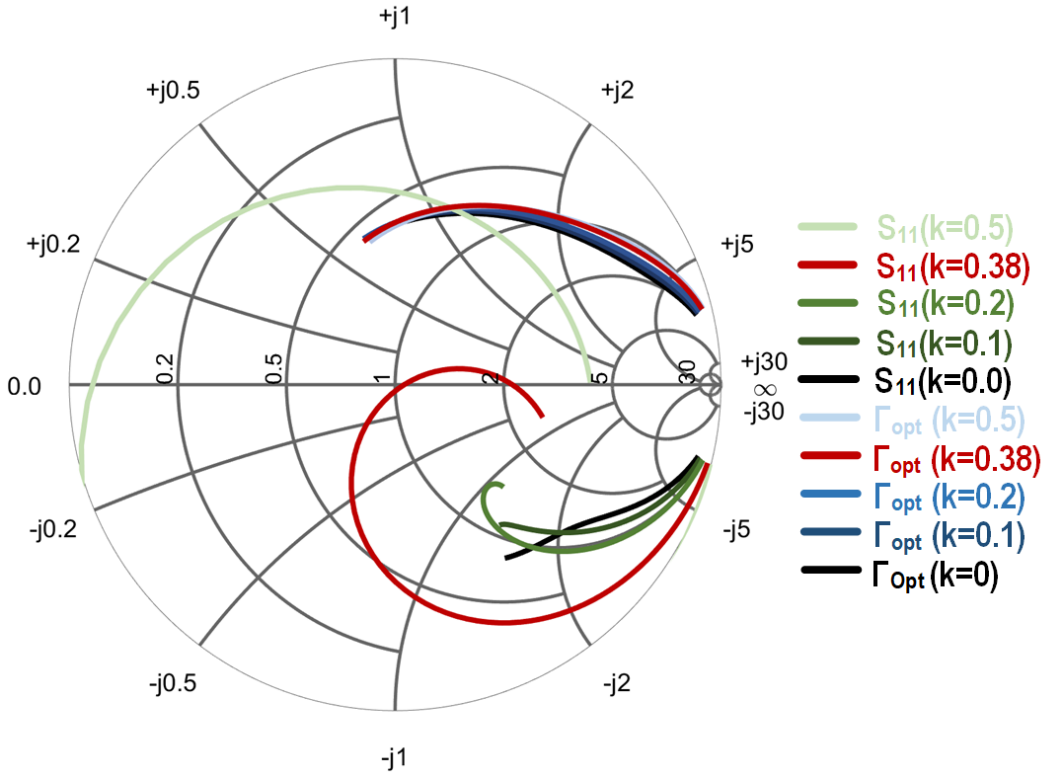
Core Transistor Optimization

- First common source transistor width is fixed at 220 µm/20nm
- Break down the large transistor into several smaller parallel transistors
  - → Improve minimum noise figure
  - → Improve associated gain
- In this design:
  - 6 unit-transistors are combined
  - Unit transistor size: 35 µm/20nm



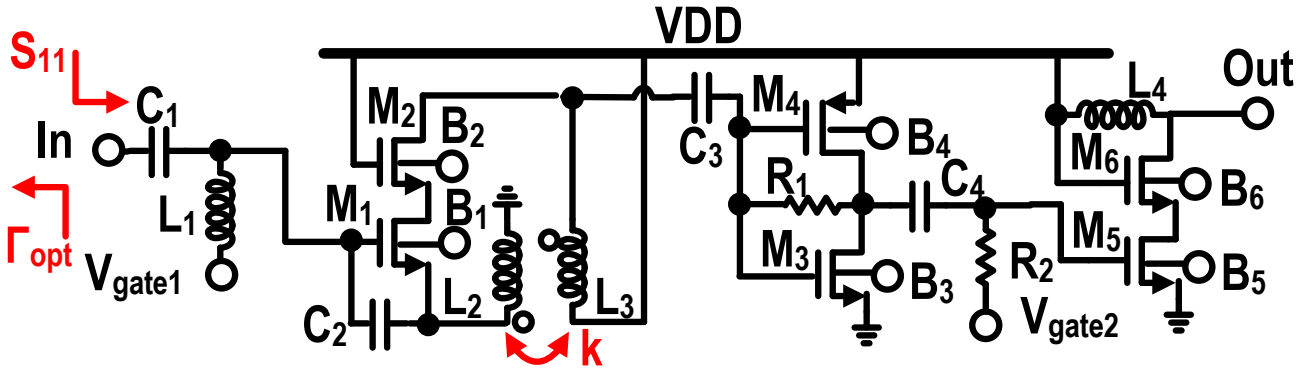
Transformer Feedback

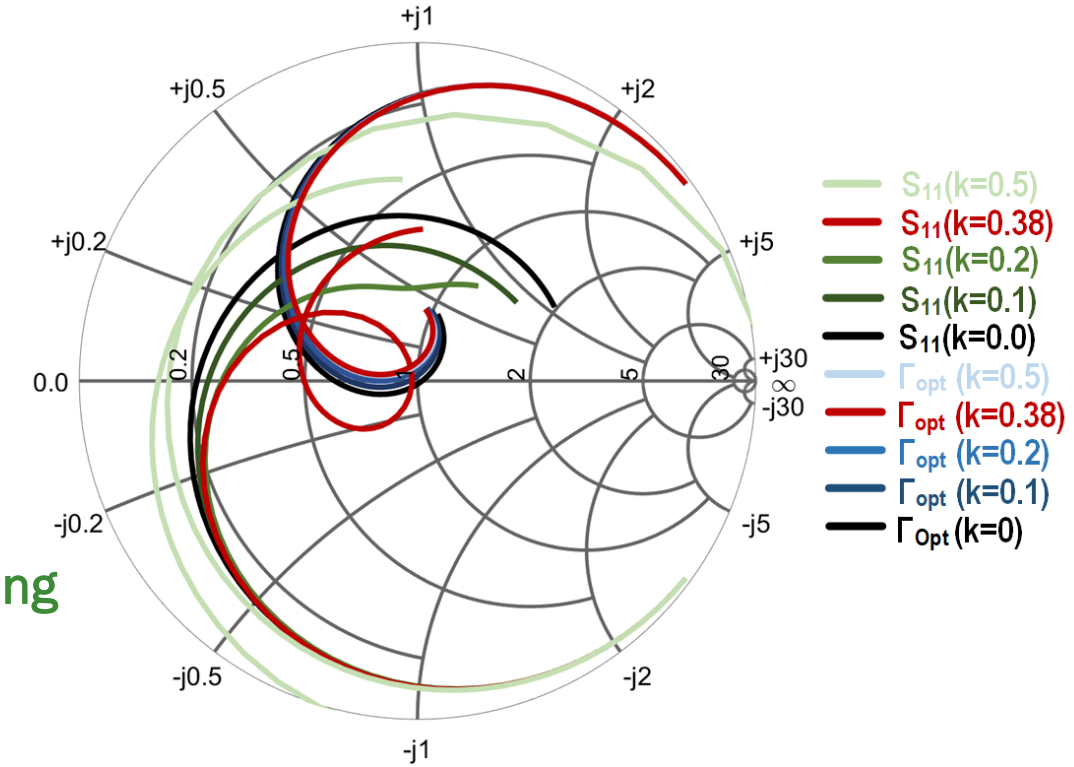




- Coupling factor (k) increase → Improve Power Matching
- Strongly coupled drain and source → Unstable Amplifier
- Optimum noise refection coefficient (Γ_{opt}) remains nearly unchanged

Transformer Feedback





- Add input matching network
  - → Achieve broadband simultaneous noise-power matching
  - → Add loss which degrades total noise figure
- Broadband power and noise matching can be achieved by properly chosen k and input matching network

Cryogenic Applications

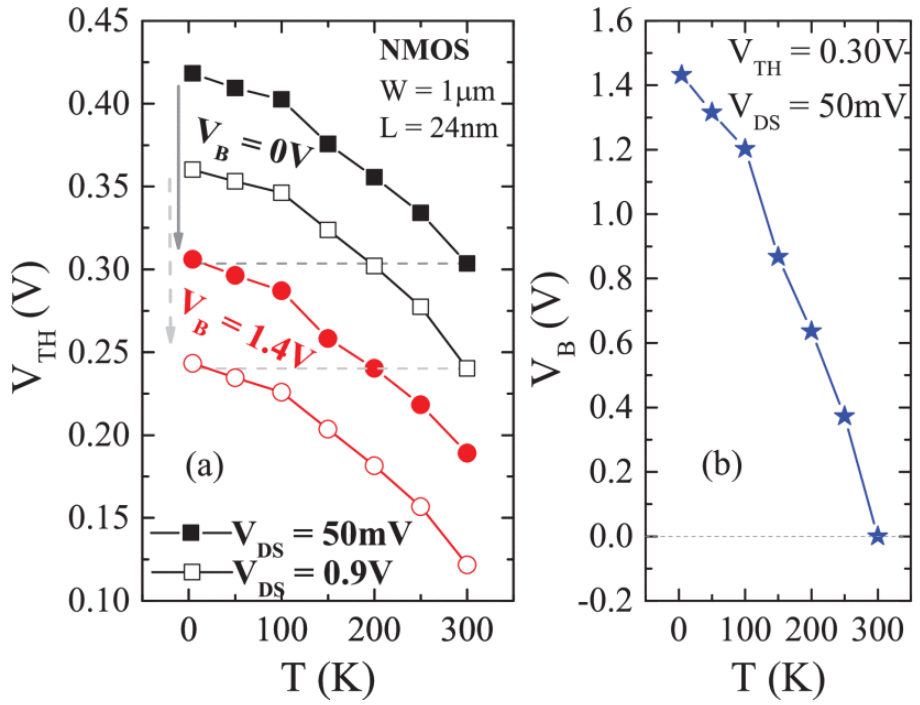
- Based on [7], the following changes are considered to design the active devices at cryogenic temperature:
  - Increase threshold voltage (V_{th})

    → Apply backgate bias can shift the $V_{th,cryo} = V_{th,RT}$
  - Increase the effective mobility due to the suppression of phonon scattering contribution

    → Affects power matching conditions

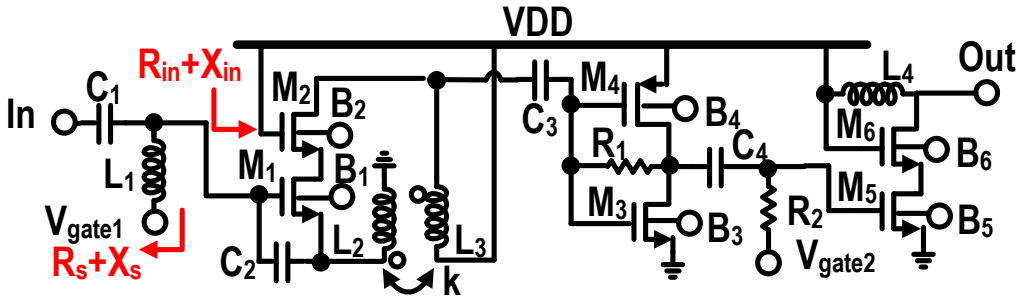
    → Simulate the response with increased gm

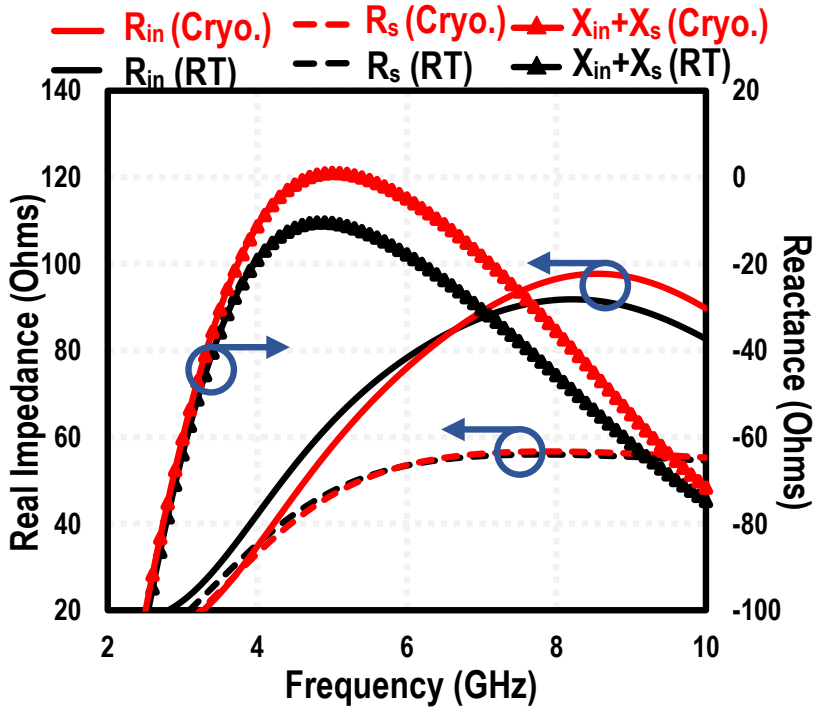
[7] Paz, et al., IEEE TED, 2020



Cryogenic Applications

- Based on [8], the following changes are considered to design the passive EM components at cryogenic temperature:
  - Metal conductivity increases five-folds
    → Metal Impurity
  - The substrate resistivity increases 1000x
    → Carrier Freeze-Out Effect





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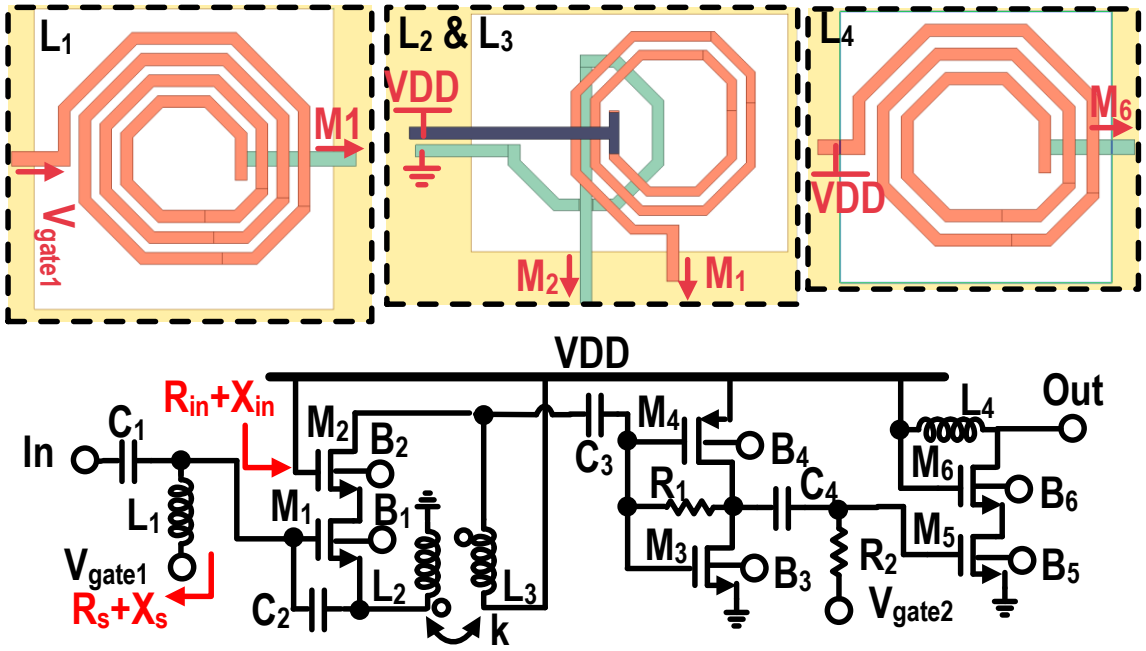
Circuit Schematic

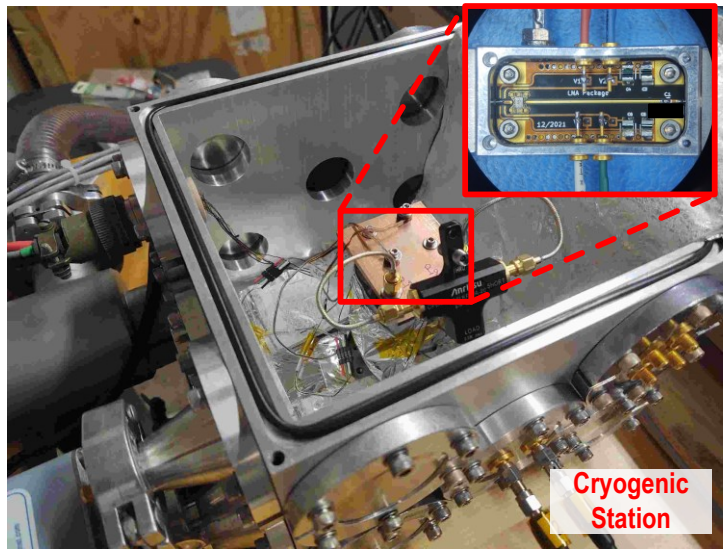
- The implemented circuit schematic and components values



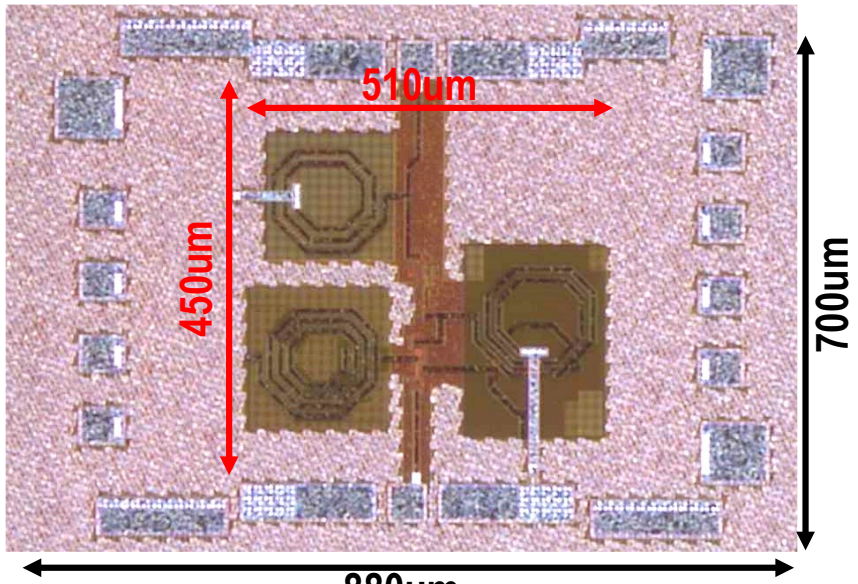
L_1	L_2	L_3	L_4	C_1
1.05nH	300pH	1.15nH	1nH	1pF
C_2	C_3	C_4	R_1	R_2
200fF	1pF	1pF	350Ω	1KΩ
k	M_1	$M_{2\text{-}3}$, $M_{5\text{-}6}$	M_4	Vdd
0.38	35μm/20nm x6	60μm/20nm	80μm/20nm	0.8V

Measurement

- The design is implemented in GlobalFoundries 22nm FDSOI CMOS technology
- The chip is packaged in a custom designed chassis within the cryogenic station



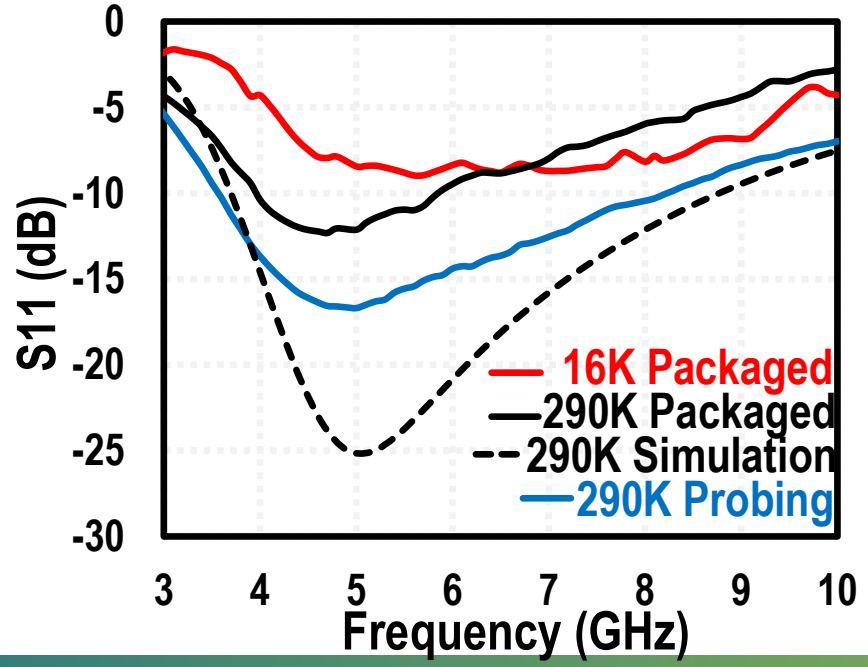
Cryogenic Measurement Setup

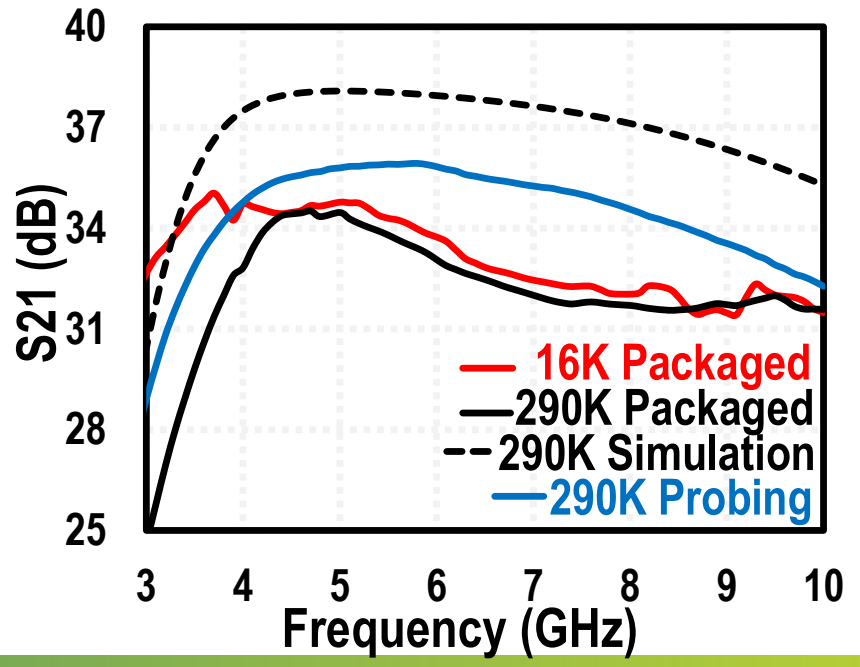


Chip Microphotograph

Measurement

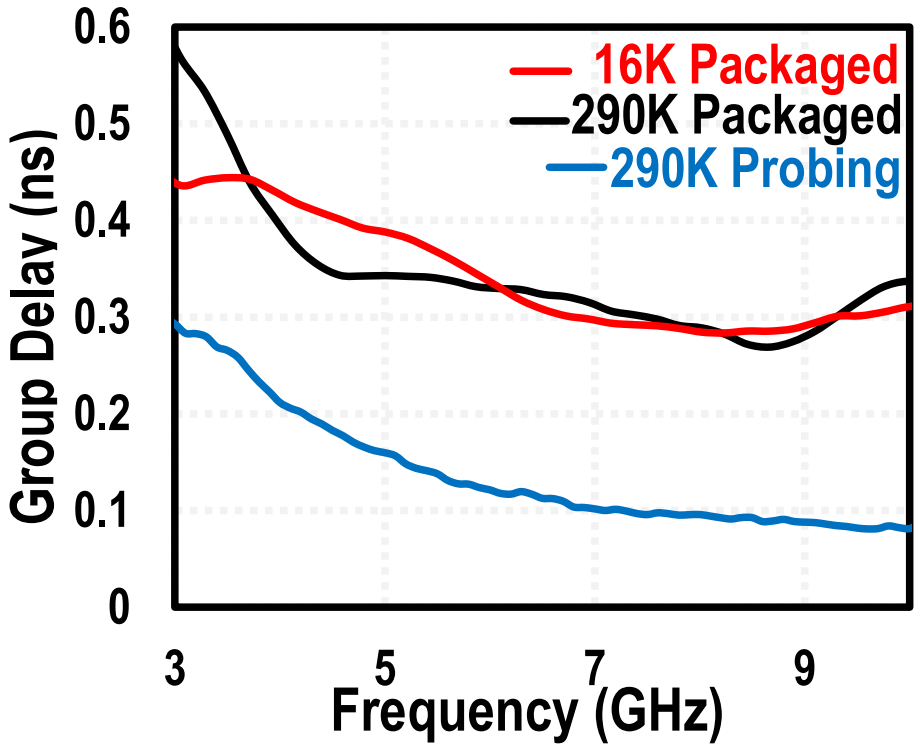
- The design is measured at 16K and 300K
- At 300K, S_{11}<-10dB from 3.6GHz to 8.2GHz with 34~35.9dB gain
- At 16K, S_{11}<-5.6dB from 4.2GHz to 9.2GHz with 31.4~34.7dB gain

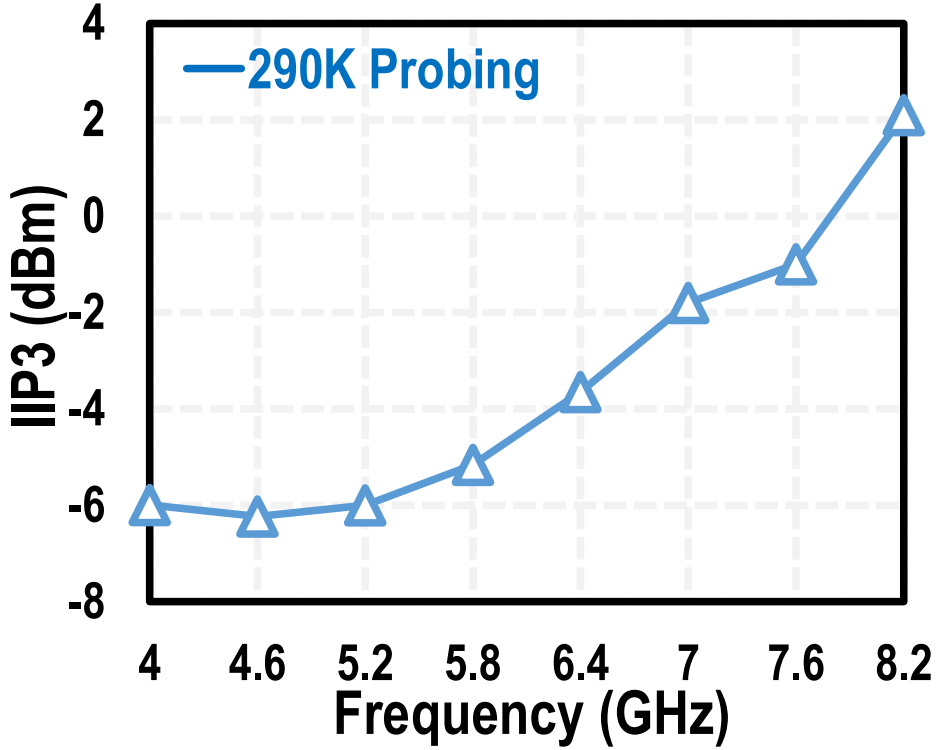




Measurement

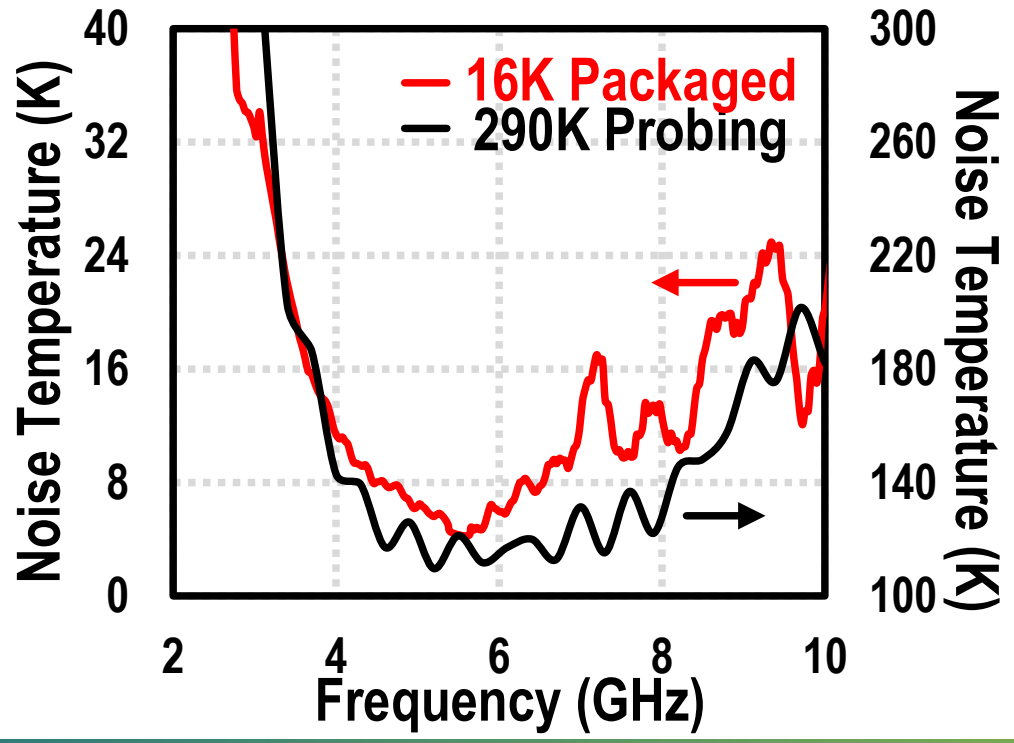
- At 300K, the total group delay is less than 0.3ns and IIP_3 > -6dBm
- At 16K, the total group delay is less than 0.42ns

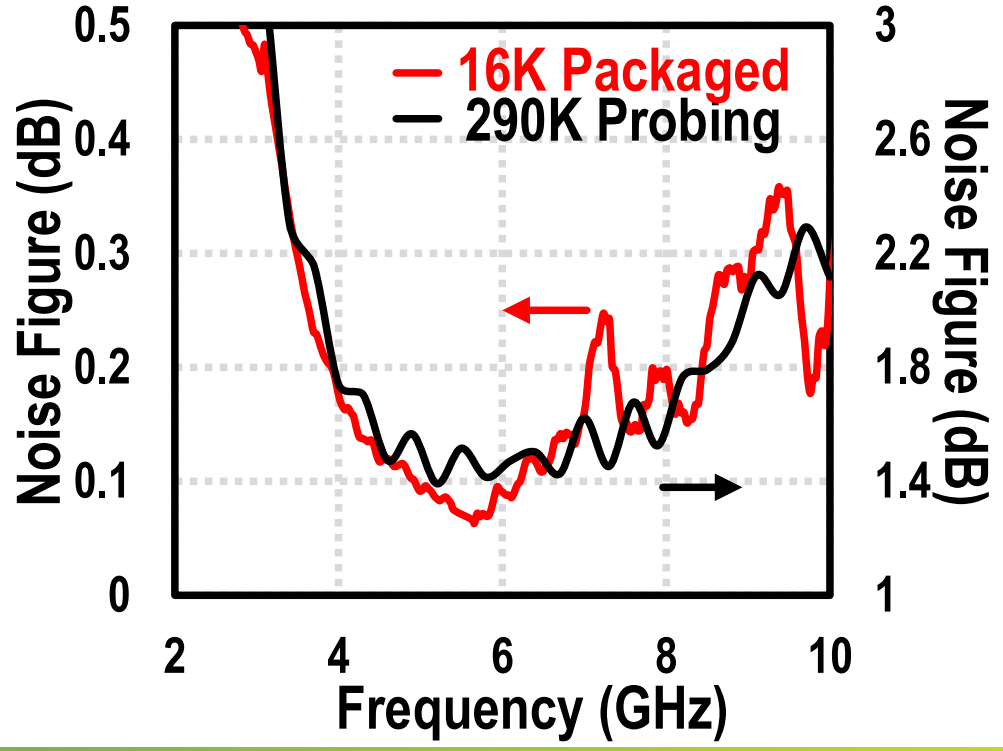




Measurement

- At 300K, the measured noise temperature is 115.1 ~153K (1.41dB~1.79dB)
- At 16K, the measured noise temperature is 4.5~21.5K (0.065dB~0.3dB)





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Comparison Table

	This Work		JSSC '21 [4]		TMTT '18 [1]		TCS '19[2]		JSSC '18[9]	
Topology	SNPM + XFMR FB + Current Reuse + Cascode		Cascode +R-C loading + XFMR load		3 Stage Cascade		Cascode CS		Noise Cancelling	
Vdd (V)	0.8		1.4		2		1.8		1.4	
Frequency (GHz)	3.6~8.2	4.2~9.2	4.1~7.9	4.6~8.2	0.3~14		2.0~2.12		0.1~0.5	
Meas. Temp. (K)	300	16†	300	4.2	300	4	300	77	N/A	N/A
Power (mW)	28	21	51.1	39	100	12	N/A	15	300	4.2
Gain(dB)	34~35.9	31.4~34.7	35.5~36.5	39.2~44.8	39.8 ~ 41.6	40.2 ~ 43	15	18	35~40	50~58
Noise Temp. (K)	115.1~153	4.5~21.5	54.7~101.2	16.3~48.4	60.7~125	2.2~13	121.5~159.2	35.4	35.4 ~ 96.7	6.8~62.7
NF (dB)^	1.41~1.79	0.065~0.3	0.73~1.26	0.23~0.65	0.80 ~ 1.51	0.03 ~ 0.18	1.52 ~ 1.9	0.48	0.8 ~ 1.25	0.1 ~ 0.85
S11 (dB)	-16.7~-10.2	-8.9~-5.6	-22~-12	-26~-5.8	-22~-1	-22 ~ -6	-10 ~ -6	-40 ~ -15	-9 ~ -5	-7 ~ -3
Area (mm^2)	0.23*		0.72		1.5		N/A		0.249	
Technology	22nm CMOS FDSOI		40nm CMOS		100nm InP HEMT		0.18µm CMOS		0.16µm CMOS	

†: Temperature is limited by testing equipment. *: Core Area. ^: NF is referring to 300K

Summary

- The implemented cryogenic CMOS LNA provide wideband 4.2GHz to 9.2GHz operation bandwidth for quantum applications.
- The implemented LNA provides broadband simultaneous noise and power matching using transformer feedback at cryogenic temperature.
- It paves the way for future quantum applications with large scale qubits integration

Acknowledgement

- Amy STTR program for sponsoring this design
- Dr. Joe Qiu for supporting this design
- GlobalFoundries for chip fabrication
- Members at Georgia Tech GMES lab for technical discussion

Reference

[1] C.-C. Chiong, et al., “Low-Noise Amplifier for Next-Generation Radio Astronomy Telescopes: Review of the State-of-the-Art Cryogenic LNAs in the Most Challenging Applications,” IEEE Microw Mag, vol. 23, no. 1, pp. 31–47, 2022, doi: 10.1109/mmm.2021.3117318.

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